2023 Digital IC Design Homework 3

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| --- | --- | --- | --- | --- | --- |
| NAME | 黃彥承 | | | | |
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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
|  | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 727 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 1 | | |
| Total cycle used | | | 2221 | | |
| Clock width | | | 20 ns | | |
| (your flow summary) | | | | | |
| **Description of your design** | | | | | |
|  | | | | | |

*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**